COMBINED TRANSMITTAL OF APPEAL BRIEF TO THE BOARD OF PATENT APPEALS AND INTERFERENCES & PETITION FOR EXTENSION OF TIME UNDER 37 C.F.R. 1.136(a) (Large Entity)	Docket No. OKI.234

In Re Application Of: **Shinji Ohuchi et al.**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
09/852,847	May 11, 2001	M. Lewis		2822	5682

Invention: **A SEMICONDUCTOR IC DEVICE HAVING A SEALED BACK SIDE**

COMMISSIONER FOR PATENTS:

This is a combined Transmittal of Appeal Brief to the Board of Patent Appeals and Interferences and petition under the provisions of 37 CFR 1.136(a) to extend the period for filing an Appeal Brief.

Applicant(s) hereby request(s) an extension of time of (check desired time period):

☐ One month ☒ Two months ☐ Three months ☐ Four months ☐ Five months

from: **February 28, 2005** (*Date*) until: **April 29, 2005** (*Date*)

The fee for the Appeal Brief and Extension of Time has been calculated as shown below:

Fee for Appeal Brief:	$500.00
Fee for Extension of Time:	$450.00
TOTAL FEE FOR APPEAL BRIEF AND EXTENSION OF TIME:	**$950.00**

The fee for the Appeal Brief and extension of time is to be paid as follows:

☒ A check in the amount of **$950.00** for the Appeal Brief and extension of time is enclosed.

☐ Please charge Deposit Account No. in the amount of

☒ The Director is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. **50-0238**

☒ Any additional filing fees required under 37 C.F.R. 1.16.

☒ Any patent application processing fees under 37 CFR 1.17.

05/02/2005 SSESHE1 00000034 09852847
02 FC:1252 450.00 OP

☒ If an additional extension of time is required, please consider this a petition therefor and charge any additional fees which may be required to Deposit Account No. **50-0238** .

☐ Payment by credit card. Form PTO-2038 is attached.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

COMBINED TRANSMITTAL OF APPEAL BRIEF TO THE BOARD OF PATENT APPEALS AND INTERFERENCES & PETITION FOR EXTENSION OF TIME UNDER 37 C.F.R. 1.136(a) (Large Entity)	Docket No. OKI.234

In Re Application Of: **Shinji Ohuchi et al.**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
09/852,847	May 11, 2001	M. Lewis		2822	5682

Invention: **A SEMICONDUCTOR IC DEVICE HAVING A SEALED BACK SIDE**

TO THE COMMISSIONER FOR PATENTS:

This combined Transmittal of Appeal Brief to the Board of Patent Appeals and Interferences and petition for extension of time under 37 CFR 1.136(a) is respectfully submitted by the undersigned:

Signature

Dated: **April 29, 2005**

ANDREW J. TELESZ, JR.
REG. NO. 33,581

VOLENTINE FRANCOS & WHITT, P.L.L.C.
ONE FREEDOM SQUARE
11951 FREEDOM DRIVE, SUITE 1260
RESTON, VA 20190
TEL. NO. (571) 283-0720

Certificate of Transmission by Facsimile*

I certify that this document and authorization to charge deposit account is being facsimile transmitted to the United States Patent and Trademark Office (Fax no.) on

_____
(Date)

Signature

Typed or Printed Name of Person Signing Certificate

***This certificate may only be used if paying by deposit account.**

Certificate of Mailing

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)] on

_____.
(Date)

Signature of Person Mailing Correspondence

Typed or Printed Name of Person Mailing Correspondence

cc:

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent application of	:	
Shinji Ohuchi	:	Group Art Unit: 2822
Serial No. 09/852,847	:	Examiner : M. Lewis
Filed: May 11, 2001	:	Confirm. No.: 5682

For: A SEMICONDUCTOR IC DEVICE HAVING A SEALED BACK SIDE

APPEAL BRIEF

U.S. Patent and Trademark Office
Customer Window, **Mail Stop Appeal Brief – Patents**
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Sir:

In response to the FINAL Office Action dated June 30, 2004, and further responsive to the Notice of Appeal filed on December 29, 2004, this corresponding Appeal Brief is respectfully submitted.

Real Party in Interest

This application is assigned to Oki Electric Industry Co., Ltd., which is the real party in interest.

Related Appeals and Interferences

There are no other appeals or interferences that will directly affect or be affected by or have a bearing on the Board's decision in this pending appeal.

Status of Claims

Claims 1-17 (canceled).

Claims 18-29 (rejected).

Claims 18-29 have been finally rejected. Accordingly, claims 18-29 are being appealed.

Status of Amendments

Subsequent to the Final Office Action dated June 30, 2004, an AMENDMENT and/or RESPONSE Under 37 C.F.R. 1.116 was filed on November 1, 2004. In the AMENDMENT and/or RESPONSE Under 37 C.F.R. 1.116 filed on November 1, 2004, claim 27 was canceled. Previously presented claims 18-26, 28 and 29 were maintained without amendment.

As indicated in the subsequent Advisory Action dated December 3, 2004, the request for reconsideration filed November 1, 2004, was considered, but did not place the application in condition for allowance.

The Advisory Action dated December 3, 2004 however did not indicate the status of the proposed Amendment filed November 1, 2004, as either entered or not entered, for the purposes of appeal. Since the Amendment Under 37 C.F.R. 1.116 filed November 1, 2004, has not been entered, the status of claim 27 as noted above is indicated as rejected. **However, Appellants respectfully request entry of the Amendment filed November 1, 2004, to thereby cancel claim 27 and materially reduce the issues for appeal**.

Summary of Claimed Subject Matter

The present invention is directed to a semiconductor device having a bump electrode and re-wiring disposed at a side surface thereof, and including an outer electrode formed on and in contact with the bump electrode and the re-wiring.

Accordingly, the invention, as broadly featured in independent claim 18, includes in combination a semiconductor element 101 having a circuit forming surface (upper side) (e.g., page 9, lines 15-17 and as shown in Figs. 1, 3 and 4) and a parallel confronting surface (back side) (e.g., page 9, line 25 and as shown in Figs. 1, 3 and 4). A wiring 104 (Cu re-wiring) is disposed on the circuit forming (upper) surface of semiconductor element 101 (e.g., page 9, lines 17-21 and as shown in Figs. 1 and 3) as connected to electrode pad 106 and as extending on a side surface of semiconductor element 101 (e.g., page 10, lines 25-26 and as shown in Figs. 1 and 3). A sealed bump electrode 102 (Cu post) is formed above the circuit forming surface of semiconductor element 101 as connected to wiring 104 (e.g., page 9, lines 19-21 and as shown in Figs. 1 and 3), wherein the sealed bump electrode 102 is sealed with a resin 105 so that a surface of the sealed bump electrode 102 is exposed from resin 105 (e.g., page 9, lines 21-23 and as shown in Figs. 1 and 3). An outer electrode 103 (solder ball) is disposed on the exposed surface of sealed bump electrode 102 (e.g., page 9, lines 23-24 and as shown in Figs. 1 and 3), wherein the outer electrode 103 also contacts wiring 104 on the side surface

of semiconductor element 101 (e.g., page 13, lines 9-12 and as shown in Figs. 1, 3 and 7(c)). Also, the parallel confronting surface or back side of semiconductor element 101 is sealed with resin 105 (e.g., page 10, lines 26-27 and as shown in Figs. 1, 3 and 4).

As broadly featured in dependent claim 20, wiring 104 on the side surface of semiconductor element 101 has an end that is sealed with resin 105 (e.g., page 9, line 25 through to page 10, line 1 and as shown in Figs. 1 and 3). That is, the bottom horizontal surface or end of wiring 104 is sealed with resin 105.

As broadly featured in claim 21, sealed bump electrode 102 (e.g., page 9, lines 21-23 as shown in Figs. 1 and 3), and the sealed confronting surface (back side) of semiconductor element 101 (e.g., page 9, line 25 through to page 10, line 1 and as shown in Figs. 1 and 3), are sealed with resin 105.

As broadly featured in claim 22, the sealed confronting surface of semiconductor element 101 is entirely sealed (e.g., page 9, line 25 through to page 10, line 1 and as shown in Fig. 1).

Grounds of Rejection to be Reviewed on Appeal

The issues on Appeal are:

(1) The rejection of claims 21 and 22 under 35 U.S.C. 112, second paragraph, as having insufficient antecedent basis;

(2) The rejection of claims 18-20 and 22-26 under 35 U.S.C. 103(a) as being unpatentable over Applicants' prior art drawings (Fig. 21) in view of the Eide reference (U.S. Patent No. 5,313,096); and

(3) The rejection of claims 21, 28 and 29 under 35 U.S.C. 103(a) as being unpatentable over Applicants' prior art drawings (Fig. 21) in view of the Eide reference (U.S. Patent No. 5,313,096) and the Mori reference (U.S. Patent No. 5,903,049).

Arguments

1) Claims 21 and 22 are in Compliance with 35 U.S.C. 112, second paragraph

Claim 21

Claim 21, as dependent upon claim 18, features "said sealed confronting surface". Claim 18 features "wherein said parallel confronting surface is sealed". One of ordinary skill would readily understand that the parallel confronting surface of claim 18 that is sealed, provides antecedent for "said sealed confronting surface" of claim 21. Appellants therefore respectfully submit that claim 21 is in compliance with 35 U.S.C. 112, second paragraph.

Claim 22

Claim 22, as dependent upon claim 18, features "said sealed confronting surface". Claim 18 features "wherein said parallel confronting

surface is sealed". One of ordinary skill would readily understand that the parallel confronting surface of claim 18 provides antecedent for "said sealed confronting surface" of claim 22. Appellants therefore respectfully submit that claim 22 is in compliance with 35 U.S.C. 112, second paragraph.

2) Claims 18-20 and 22-26 Are Patentable Over The Combination of Applicants' Prior Art Drawings In View Of The Eide Reference

Claims 18-20 and 22-26 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' prior art drawings (Fig. 21) in view of the Eide reference. This rejection is respectfully traversed for at least the following reasons.

Claim 18

The semiconductor device of claim 18 includes in combination a semiconductor element; a wiring "disposed on said circuit forming surface and on a side surface of said semiconductor element"; a sealed bump electrode "connected to said wiring, said sealed bump electrode having an exposed surface"; an outer electrode "disposed on said exposed surface of said bump electrode and contacting said wiring on said side surface of said semiconductor element"; and wherein said parallel confronting surface is sealed. Appellants respectfully submit that the prior art as relied upon by the Examiner does not make obvious these features.

On page 3 of the Final Office Action dated June 30, 2004, the Examiner has acknowledged that Applicants' prior art drawings (Fig. 21) fail to disclose a sealed parallel confronting (back side) surface.

In order to overcome this acknowledged deficiency of Applicants' prior art, the Examiner has alleged that "However, Eide discloses a sealed confronting surface (For Example: See Figure 2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art Drawings to include a sealed confronting surface as disclosed in Eide because it aids in providing high chip density (For Example: See Column 8 Lines 34 and 35)". Appellants respectfully disagree for the following reasons.

Appellants respectfully submit that the Examiner has failed to specifically identify on the record how Fig. 2 of the Eide reference may be interpreted to include a "**sealed** confronting surface", as would be necessary to meet the features of claim 18. As described beginning in column 4, line 18 of the Eide reference with respect to Figs. 1 and 2, chip stack 10 includes a plurality of chip packages 12. As further described in column 4, lines 31-41 of the Eide reference with respect to Fig. 2, each chip package 12 is comprised of an IC chip or die 20 disposed beneath a substrate 22. Substrate 22 is multilayer in nature and is comprised of a lower substrate layer 24 disposed immediately above and attached to chip 20, and is further comprised of an upper substrate layer 26 disposed over lower substrate layer 24. Chip 20 of

each chip package 12 is disposed on top of upper substrate layer 26 of chip package 12 immediately therebelow.

Appellants respectfully submit that Figs. 1 and 2 of the Eide reference are not specifically described in column 4, lines 18-59 as having a "**sealed** confronting surface" as asserted by the Examiner. On the contrary, upper and lower substrate layers 24 and 26 in Figs. 1 and 2 of the Eide reference are described in column 4, lines 44-46 of the Eide reference as merely "joined together as part of the process of forming substrate 22, before the chip 20 is attached thereto". Chip 20, lower substrate layer 24 and upper substrate layer 26 of each chip package 12 are further described beginning in column 4, line 60 of the Eide reference with respect to Figs. 3, 4 and 5 respectively. A sealed surface is not described in the paragraph beginning in column 4, line 60 of the Eide reference.

Accordingly, a "**sealed** confronting surface" is not specifically described or even remotely suggested in the Eide reference. Particularly, a sealing resin is not specifically described or even remotely suggested in the Eide reference as relied upon by the Examiner. Column 8, lines 34 and 35 of the Eide reference as further relied upon by the Examiner does not describe or suggest a "**sealed** confronting surface". The Eide reference as relied upon by the Examiner thus fails to overcome the acknowledged deficiency of Applicants' admitted prior art (Fig. 21), as asserted by the Examiner. Appellants therefore respectfully submit that the semiconductor device of claim 18 would not have been obvious in view of the prior art as relied upon by the Examiner taken

singularly or together, and that this rejection of claim 18 is thus improper for at least these reasons.

On page 4 of the Final Office Action dated June 30, 2004, the Examiner has further acknowledged that Applicants' prior art drawings (Fig. 21) do not include an "outer electrode contacting said wiring on said side surface of said semiconductor element".

In order to overcome this additional acknowledged deficiency of Applicants' prior art drawing (Fig. 21), the Examiner has alleged that "However, Eide discloses an outer electrode (60) contacting wiring on said side surface of the semiconductor element (For Example: See Figure 2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art Drawings to include an outer electrode contacting wiring on said side surface as disclosed in Eide because it aids in coupling chip packages in parallel (For Example: See Column 4 Lines 27 and 28)". Appellants respectfully disagree for the following reasons.

Initially, for the purpose of clarifying the record, on the Advisory Action (December 3, 2004) Continuation Sheet, the Examiner has confirmed that **strips of solder 16** (as illustrated in Figs. 1 and 2 of the Eide reference) have been interpreted as the outer electrode of claim 18. This is in contrast to page 4 of the Final Office Action dated June 30, 2004, where the Examiner apparently inadvertently indicated that element 60 of the Eide reference had been interpreted as the outer electrode of claim 18. **Accordingly, the**

following remarks are submitted of record with the understanding that solder strips 16 in Figs. 1 and 2 of the Eide reference have been interpreted as the outer electrode of claim 18.

As emphasized previously, claim 18 includes in combination an outer electrode "**disposed on said exposed surface of said bump electrode** and contacting said wiring on said side surface of said semiconductor element". Appellants respectfully submit that solder strips 16 of the Eide reference cannot be interpreted as the outer electrode of claim 18, and that the prior art as relied upon by the Examiner does not make obvious the features of claim 18.

The Examiner has very generally alleged on page 4 of the Final Office Action dated June 30, 2004, that the Eide reference discloses an outer electrode (16) in Fig. 2 contacting wiring on the side surface of the semiconductor element. **However, the Examiner has not specifically explained on the record how the structure in Fig. 21 of Applicants' prior art would be modified in view of the Eide reference to meet the features of claim 18**.

As described in column 4, lines 24-27 of the Eide reference with respect to Fig. 1, "Vertical strips of solder 16 extend along side surfaces 18 of the individual chip packages 12 **to couple conductive pads** on the chip packages 12 in parallel" (our emphasis added). As further described in column 4, lines 55-59, "solder strips 16 of FIG. 1 contact the conductive film

28 and the opposite conductive pads 30 and 32 of each chip package 12, to form a vertical conductor array, as shown in FIG. 2".

Accordingly, although the Examiner has not explained exactly how the structure in Fig. 21 of Applicants' prior art would be modified in view of the Eide reference, Appellants presume that solder strip 16 and conductive film 28 of the Eide reference as incorporated into the Fig. 21 structure of Applicants' prior art, would be disposed so that a first end of conductive film 28 is coupled to electrode pad 606 and so that conductive film 28 extends downward along the sidewall of the structure to be coupled to some other corresponding electrode pad. Presumably, solder strip 16 would be disposed on conductive film 28 and electrode pad 606. This presumption should logically follow from the Eide reference, because solder strips 16 of the Eide reference are disposed as having opposite ends coupled to conductive pads 30 and 32, as shown in Fig. 2.

Appellants however respectfully submit that modification of the structure in Fig. 21 of Applicants' prior art in the above presumed manner would raise the following problems.

First, the structure in Fig. 21 of Applicants' prior art does not include electrode pads or conductive pads on the bottom surface of semiconductor element 601, opposite the upper surface having electrode pads thereon. Accordingly, there would be no reason to modify the structure in Fig. 21 of Applicants' prior art to include conductive film 28 and solder strips 16 as in the Eide reference, because additional conductive pads or electrode pads do not

exist at an underside of or at a level below semiconductor element 601 in the structure of Applicants' prior art Fig. 21. That is, one of ordinary skill would have no motivation to modify the structure in Fig. 21 of Applicants' prior art as taken alone, to include conductive film 28 and solder strip 16 as in the Eide reference.

Secondly, as noted above, the outer electrode of claim 18 is featured as "**disposed on said exposed surface of said bump electrode** and contacting said wiring on said side surface of said semiconductor element" (our emphasis added). Even if motivation existed for modifying the structure in Fig. 21 of Applicants' prior art in view of the Eide reference in the above noted presumed manner, which motivation Appellants do not admit exists, solder strip 16 would not also be "disposed on said exposed surface of said bump electrode", as would be necessary to meet the features of claim 18.

That is, conductive film 28 of the Eide reference would presumably be coupled to electrode pad 606 of the structure in Fig. 21 of Applicants' prior art as modified in view of the Eide reference, **necessarily under resin 605**. Solder strip 16 of the Eide reference would then consequently be disposed on conductive film 28 and electrode pad 606 of the structure in Fig. 21 of Applicants' prior art as modified in view of the Eide reference, **also necessarily under resin 605**.

In the Fig. 21 structure of Applicants' prior art, the only surface of bump electrode 602 that is exposed from resin 605, is covered by and thus in contact with solder ball 603. That is, the structure of Applicants' prior art Fig.

21 does not have an exposed surface of bump electrode 602 available to have a solder strip disposed thereon, because the only surface of bump electrode 602 exposed from resin 605 already has solder ball 603 disposed thereon. Also, solder strip 16 of the modified structure would necessarily be under resin 605, thus being buried and unable to be disposed on an exposed surface of bump electrode 602.

Moreover, solder strips 16 in Fig. 2 of the Eide reference are designed to be in contact with conductive pads 30 and 32, not to be in contact with bump electrodes or posts. This should be especially clear, because the structure in Figs. 1 and 2 of the Eide reference does not include bump electrodes or posts.

Appellants therefore respectfully submit that solder strip 16 of the Eide reference as combined with the structure of Applicants' Fig. 2 cannot be interpreted as the outer electrode of claim 18. The Eide reference as relied upon by the Examiner therefore does not overcome the deficiencies of Applicants' prior art. Accordingly, Appellants respectfully submit that the semiconductor device of claim 18 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claim 18 is improper for at least these additional reasons.

Claim 20

Claim 20 depends from claim 18, and should thus be deemed patentable for at least the reasons as set forth above with respect to claim 18,

and for the following additional reasons.

The semiconductor device of claim 20, as dependent upon claim 18, features that "said wiring on said side surface has an end that is sealed".

On page 4 of the final Office Action dated June 30, 2004, the Examiner has acknowledged that Applicants' prior art does not disclose the features of claim 20. In order to overcome this further acknowledged deficiency of Applicants' prior art, the Examiner has alleged that "However, Eide discloses wiring on said side surface that is sealed (For Example: See Figure 2)". The Examiner has asserted that it would have been obvious to modify Applicants' prior art Fig. 21 in view of the Eide reference "because it aids in coupling chips in parallel (For Example: See Column 4 Lines 27 and 28)".

As emphasized previously, Appellants respectfully submit that Fig. 2 of the Eide reference as relied upon by the Examiner is not specifically described or even remotely suggested as having a sealed surface or as including sealing resin. As described in column 4, lines 44-46 of the Eide reference, layers 24 and 26 are merely joined together as part of the process of forming substrate 22, before chip 20 is attached thereto. As further described in column 4, lines 55-59 of the Eide reference, solder strip 16 in Fig. 1 merely contacts the conductive film 28 and the opposite conductive pads 30 and 32 of each chip package 12.

Accordingly, since the Eide reference does not disclose sealing, and particularly does not disclose a sealing resin, the Eide reference clearly fails to disclose or even remotely suggest a wiring on a side surface that has an end

that is sealed, as asserted by the Examiner. The Eide reference as herein relied upon by the Examiner thus fails to overcome the acknowledged deficiencies of Applicants' prior art, as alleged by the Examiner. Appellants therefore respectfully submit that the semiconductor device of claim 20 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, for at least these additional reasons.

Claims 19 and 22-26

Claims 19 and 22-26 depend from claim 18, and thus should be patentable for at least the reasons as set forth above with respect to claim 18.

3) Claims 21, 28 and 29 Are Patentable Over The Combination of Applicants' Prior Art Drawings In View Of The Eide Reference And The Mori Reference

Claims 21, 28 and 29 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' prior art drawings (Fig. 21) in view of the Eide reference and the Mori reference. Appellants respectfully submit that claims 21, 28 and 29 depend from claim 18, and should thus be deemed patentable for at least the reasons as set forth above with respect to claim 18.

CONCLUSION

Appellants respectfully submit that claims 18-26, 28 and 29 would not have been obvious in view of the prior art as relied upon by the Examiner

taken singularly or together. Appellants therefore respectfully request that the final rejection of claims 18-26, 28 and 29 be withdrawn, and that these corresponding claims be passed to issue in the present application.

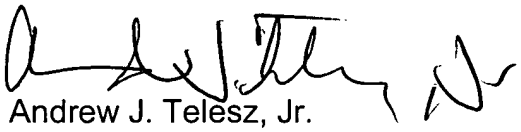
The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. 41.20, particularly extension of time fees.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



Andrew J. Telesz, Jr.
Registration No. 33,581

One Freedom Square
11951 Freedom Drive, Suite 1260
Reston, Virginia 20190
Telephone No.: (571) 283-0270
Facsimile No.: (571) 283-0740

Appendix - Claims on Appeal

18. A semiconductor device, comprising:

a semiconductor element having a circuit forming surface and a parallel confronting surface;

a wiring disposed on said circuit forming surface and on a side surface of said semiconductor element;

a sealed bump electrode connected to said wiring, said sealed bump electrode having an exposed surface;

an outer electrode disposed on said exposed surface of said bump electrode and contacting said wiring on said side surface of said semiconductor element; and

wherein said parallel confronting surface is sealed.

19. A semiconductor device as recited in claim 18, further comprising a plurality of electrodes on said circuit forming surface.

20. A semiconductor device as recited in claim 18, wherein said wiring on said side surface has an end that is sealed.

21. A semiconductor device as recited in claim 18, wherein said sealed bump electrode and said sealed confronting surface are resin sealed.

22. A semiconductor device as recited in claim 18, wherein said sealed confronting surface is entirely sealed.

23. A semiconductor device as recited in claim 18, wherein the semiconductor device is mounted on another semiconductor device with said confronting surface as a contacting surface.

24. A semiconductor device as recited in claim 23, wherein said another semiconductor device has electrodes that are connected to said wiring of the semiconductor device.

25. A semiconductor device as recited in claim 19, wherein the semiconductor device is mounted on another semiconductor device with said confronting surface as a contacting surface, and said another semiconductor device has electrodes that are connected to said wiring and to at least one of said plurality of electrodes.

26. A semiconductor device as recited in claim 23, wherein said another semiconductor device is disposed over a plurality of other semiconductor devices.

27. A semiconductor device as recited in claim 18, wherein at least a part of said outer electrode is disposed on said wiring disposed on said side surface of said semiconductor element.

28. A semiconductor device as recited in claim 18, wherein said circuit forming surface is sealed.

29. A semiconductor device as recited in claim 28, wherein said circuit forming surface and said parallel confronting surface are resin sealed.